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REMARKS

This is responsive to the Non-Final Office Action mailed August 30, 2006. In that Office Action, the Examiner rejected claims 1, 2, 4-7, 11-20 under 35 U.S.C. §102(b) as being anticipated by Webster, U.S. Patent No. 6,583,101 ("Webster"). Claims 8 and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hoshino, U.S. Patent No. 6,759,642 ("Hoshino") in view of Enquist, U.S. Patent No. 6,822,326 ("Enquist"). Claims 3 and 10 were rejected under 35 U.S.C. §103(a) as being unpatentable over Webster and Hoshino in view of Enquist.

With this Response, claim 1, 8, and 11 have been amended. Claims 1-20 remain pending in the application and are presented for reconsideration and allowance.

35 U.S.C. § 102 Rejections

The Examiner rejected claims 1, 2, 4-7, 11-20 under 35 U.S.C. §102(b) as being anticipated by Webster, U.S. Patent No. 6,583,101 ("Webster"). Amended independent claim 1 recites "wafer-level packaging enclosing the IC and formed at a semiconductor wafer level when the IC is positioned on a semiconductor wafer". There is no teaching or suggestion in Webster regarding wafer-level packaging as recited in independent claim 1. Rather, the packaging disclosed in Webster relates to the packaging of separate and discrete image sensor chips 106. (See, e.g., Webster at 1, 2, 8, 9, 11, 12, and 15-17, and corresponding description).

Amended independent claim 1 also recites "a first adjustable height spacing structure providing a cavity between an inner surface of the transparent enclosure portion and the image sensing device, wherein a depth of the cavity is configurable along an axis perpendicular to the semiconductor substrate to control a distance between an outer surface of the transparent enclosure portion and the image sensing device, and wherein the depth of the cavity is configured during assembly of the imaging module based on an adjustment of a height of the spacing structure during the assembly." Webster discloses an image sensor package 100 with a molding 124 that holds a window 122 in place over an image sensor 106. (See, e.g., Webster at

Figs. 1 and 2, and col. 6, line 55, to col. 7, line 18). There is no teaching or suggestion in Webster regarding an adjustable height spacing structure. Webster also does not teach or suggest "wherein the depth of the cavity is configured during assembly of the imaging module based on an adjustment of a height of the spacing structure during the assembly", as recited in claim 1.

In view of the above, independent claim 1 is not taught or suggested by Webster. In addition, dependent claims 2 and 4-7 which further limit patentably distinct claim 1, and are further distinguishable over the cited reference, are also believed to be allowable over the cited reference. Allowance of claims 1, 2, and 4-7 is respectfully requested.

Amended independent claim 11 recites "wafer-level packaging enclosing the IC and formed at a semiconductor wafer level when the IC is positioned on a semiconductor wafer". There is no teaching or suggestion in Webster regarding wafer-level packaging as recited in independent claim 11. Rather, the packaging disclosed in Webster relates to the packaging of separate and discrete image sensor chips 106. (See, e.g., Webster at 1, 2, 8, 9, 11, 12, and 15-17, and corresponding description).

Amended independent claim 11 also recites that the wafer-level packaging includes "a packaging substrate, wherein the semiconductor substrate is positioned over the packaging substrate and extends over substantially an entire top surface of the packaging substrate". Webster discloses an image sensor 106 positioned over a substrate 102. (See, e.g., Webster at Fig. 2). However, the image sensor 106 disclosed in Webster does not extend over substantially an entire top surface of substrate 102.

Amended independent claim 11 further recites "a transparent enclosure portion extending over substantially an entire top surface of the packaging substrate". Webster discloses a window 122 positioned over a substrate 102. (See, e.g., Webster at Fig. 2). However, the window 122 disclosed in Webster does not extend over substantially an entire top surface of substrate 102.

In view of the above, independent claim 11 is not taught or suggested by Webster. In addition, dependent claims 12-20 which further limit patentably distinct claim 11, and are further distinguishable over the cited reference, are also believed to be allowable over the cited reference. Allowance of claims 11-20 is respectfully requested.

35 U.S.C. §103 Rejections

Claims 8 and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hoshino, U.S. Patent No. 6,759,642 ("Hoshino") in view of Enquist, U.S. Patent No. 6,822,326 ("Enquist"). Amended independent claim 8 is directed to a method of fabricating integrally packaged imaging modules, and recites "forming an array of integrated circuits (ICs) on a semiconductor wafer, each IC including an image sensing device" and "integrally packaging the array of ICs on the wafer with wafer-level packaging". There is no teaching or suggestion in Hoshino regarding packaging an array of image sensing devices on a wafer with wafer-level packaging. Rather, the packaging disclosed in Hoshino relates to the packaging of a discrete image pickup device 11 or 55. (See, e.g., Hoshino at Figures 2, 4, and 6, and corresponding description). There is also no teaching or suggestion in Enquist regarding fabricating integrally packaged imaging modules, or packaging an array of image sensing devices on a wafer with wafer-level packaging. Enquist does not appear to even mention an imaging module, image sensor, image sensing device, image sensing array, array of imaging sensing devices, etc. There is no teaching or suggestion in Enquist that any of the techniques disclosed therein could or should be applied to an array of imaging sensing devices. There is no teaching or suggestion in Enquist regarding the fabrication of integrally packaged imaging modules.

Amended independent claim 8 also recites that the packaging step comprises "enclosing the array of ICs on a first side with a continuous transparent enclosure layer so that each image sensing device of each IC in the array on the wafer can detect an image consisting of a desired range of wavelengths through the transparent enclosure layer". The Examiner appeared to acknowledge that Hoshino does not teach or suggest this limitation of claim 8. (See, e.g., Office Action at para. no. 7, page 4, stating that "Hoshino does not disclose to place a continuous transparent enclosure over the entire ICs"). Enquist also does not teach or suggest this limitation. As mentioned above, Enquist does not appear to even mention an imaging module, image sensor, image sensing device, image sensing array, array of imaging sensing devices, etc. There is no teaching or suggestion in Enquist that any of the techniques disclosed therein could or should be applied to an array of imaging sensing devices. In addition, Enquist discloses that "cover 8 is shown as transparent for ease of illustrating the devices 2, **but will be opaque in the usual case**, such as a silicon cover." (Enquist at col. 5, lines 51-53) (emphasis added). Enquist does not teach or suggest "enclosing the array of ICs on a first side with a continuous transparent enclosure layer so that each image sensing device of each IC in the array on the wafer can detect an image consisting of a desired range of wavelengths through the transparent enclosure layer", as recited in independent claim 8.

Amended independent claim 8 also recites that the packaging step comprises "aligning and attaching an array of lens supports to another packaging layer of the wafer such that lenses used with the array of lens supports are optically aligned with corresponding image sensing devices". There is no teaching or suggestion in Hoshino or Enquist regarding an **array** of lens supports, or attaching such an array to a packaging layer of a semiconductor wafer.

Amended independent claim 8 further recites "dicing the packaged array of ICs on the wafer into individual integrally packaged imaging modules." There is no teaching or suggestion in Hoshino or Enquist regarding dicing a packaged array of ICs on a semiconductor wafer into individual integrally packaged imaging modules.

In addition, there is no suggestion to combine the cited references. The Federal Circuit has stated "[i]n holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in the way that would produce the claimed invention" *Karsten Manufacturing Corp. vs. Cleveland Golf Co.*, 58 U.S.P.Q.2d 1286, 1293 (CAFC 2001). Hoshino discloses a package for a discrete image pickup device 11 or 55. (See, e.g., Hoshino at Figures 2, 4, and 6, and corresponding description). In contrast, Enquist discloses a wafer level encapsulation. (See, e.g., Enquist at Title and Abstract). Wafer level processes occur at different times, use different equipment, and involve many different parameters and issues than the processing of a discrete device. There is no teaching or suggestion in Hoshino that the techniques for the discrete image pickup device disclosed therein could or should be applied to an encapsulated wafer, such as that disclosed in Enquist. There is

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no teaching or suggestion in Enquist that the wafer level techniques disclosed therein could or should be applied to a discrete image pickup device, such as that disclosed in Hoshino.

In view of the above, independent claim 8 is not taught or suggested by Hoshino and Enquist. In addition, dependent claim 9 which further limits patentably distinct claim 8, and is further distinguishable over the cited references, is also believed to be allowable over the cited references. Allowance of claims 8 and 9 is respectfully requested.

Claims 3 and 10 were rejected under 35 U.S.C. §103(a) as being unpatentable over Webster and Hoshino in view of Enquist. Dependent claims 3 and 10, which further limit patentably distinct claims 1 and 8, respectively, and are further distinguishable over the cited references, are believed to be allowable over the cited references. Allowance of claims 3 and 10 is respectfully requested.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-20 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-20 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-3718.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to either Jeff A. Holmen at Telephone No. (612) 573-0178, Facsimile No. (612) 573-2005 or Michael A. Goodwin at Telephone No. (303) 298-9888, Facsimile No. (303) 297-2266. In addition, all correspondence should continue to be directed to the following address:

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CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being facsimile transmitted to the United States Patent and Trademark Office, Fax No. (571) 273-8300 on this 28th day of September, 2006.

By:
Name: Jeff A. Holmen